CLAIMS

1. A memory system comprising:
a first memory device;
a second memory device stacked on the first memory device; and
a buffer coupled to the first and second memory devices.

2. A memory system according to claim 1 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

3. A memory system according to claim 1 further comprising a bus coupled to the buffer.

4. A memory system according to claim 3 further comprising a memory controller coupled to the bus.

5. A memory system according to claim 1 wherein the buffer is a first buffer and further comprising:
a third memory device;
a fourth memory device stacked on the third memory device; and
a second buffer coupled to the third and fourth memory devices and to the first buffer.

6. A memory system according to claim 5 wherein the first buffer is adapted to receive a signal and redrive the signal to the second buffer.

7. A memory system according to claim 5 wherein the first buffer is adapted to receive a plurality of signals and redrive the plurality of signals to the second buffer.

8. A memory system according to claim 5 further comprising a memory controller coupled to the first buffer.

5. A memory system according to claim 4 wherein the memory controller, the first buffer, and the second buffer are coupled together in a multi-drop arrangement.

6. A memory system according to claim 4 wherein the memory controller, the first buffer, and the second buffer are coupled together in a point-to-point arrangement.

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11. A memory module comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus.

12. A memory module according to claim 11 further comprising a connector attached to the module and adapted to couple the module to a bus.

8. A memory module according to claim 7 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

14. A memory module according to claim 11 wherein the memory module is adapted to receive a signal from the bus and to redrive the signal to another memory module.

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15. A memory module according to claim 11 wherein the memory module is adapted to receive a plurality of signals from the bus and to redrive the plurality of signals to another memory module.

16. A memory module according to claim 11 wherein the buffer is adapted to receive a signal from the bus and to redrive the signal to another memory module.

17. A memory system comprising:

a bus;

a stack of memory devices; and

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a buffer coupled between the stack of memory devices and the memory bus.

18. A memory system according to claim 17 further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus.

19. A memory system according to claim 17 wherein the buffer is a first buffer and further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

20. A memory system according to claim 17 further including a memory controller coupled to the bus.

21. A memory system according to claim 17 wherein the stack of memory devices is mounted on a memory module.

22. A memory system according to claim 21 wherein the buffer is mounted on the memory module.

23. A memory system according to claim 21 wherein the bus is fabricated on a circuit board and the buffer is mounted on the circuit board.